Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**Pad Function**

1. **A**0
2. **B**0
3. **O**0
4. **A**1
5. **B**1
6. **O**1
7. **GND**
8. **0**3
9. **B**3
10. **A**3
11. **O**2
12. **B**2
13. **A**2
14. **Vcc**

**.033”**

**.035”**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**6 7 8**

**1 14 13**

**A**

**M**

**0**

**0**

**8**

**T**

**DIE ID**

**A**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .034” X .036” DATE: 2/2/23**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54F08**

**DG 10.1.2**

#### Rev B, 7/19/02